Patent claims

1. A receiver, in particular a clock receiver circuit device (1) with a first input (9a) adapted to be connected with a first connection (3a) of a semi-conductor component, and second input (8a) adapted to be connected with a second connection (3b) of the semi-conductor component,

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the receiver circuit device (1) comprises several, in particular more than three transfer gates (4, 5, 6, 7).

2. A receiver circuit device (1) according to Claim 1, which comprises four transfer gates (4, 5, 6, 7).

3. A receiver circuit device (1) according to Claim 1 or 2, in which at a first transfer gate (5) a corresponding first transfer gate control input is connected with the second input (8a) of the receiver circuit device (1), and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with the first input (9a) of the receiver circuit device (1).

4. A receiver circuit device (1) according to Claim 3, in which at a second transfer gate (4) - connected with the first transfer gate (5) - a corresponding first transfer gate control input is connected with the first input (9a) of the receiver circuit device (1), and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input is connected with the second input (8a) of the receiver circuit device (1).

5. A receiver circuit device (1) according to one of the preceding claims, in which at a third transfer gate (7) a corresponding first transfer gate control input is connected with the first input (9a) of the receiver circuit device (1), and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input is connected with the second input (8a) of the receiver circuit device (1).

6. A receiver circuit device (1) according to Claim 5, in which at a fourth transfer gate (6) - connected with third transfer gate (7) - a corresponding first transfer gate control input is connected with the second input (8a) of the receiver circuit device (1), and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with first input (9a) of the receiver circuit device (1).

7. A receiver circuit device (1) according to one of the above claims, in which differential clock signals (clk, bclk) are present at the first and second inputs (9a, 8a).

8. A receiver circuit device (1) according to one of the claims 4 to 7, in which the signal (bout) - detectable between the first and second transfer gates (4, 5) - and/or the signal (out) - detectable between the third and fourth transfer gates (7, 6) - is used to boost a clock relaying circuit (2).

9. A clock receiver circuit device (1) with a first clock input (9a) for receiving a first clock signal (clk), and a second clock input (8a) for receiving a second clock signal (bclk), inversely equal to the first clock signal (clk)

- whereby at a first transfer gate (5) a corresponding first transfer gate control connection is connected with the second clock input (8a) of the clock receiver circuit device (1), and a corresponding second transfer gate control connection, inverse in relation to the first transfer gate control connection, with the first clock input (9a) of the clock receiver circuit device (1),
- and whereby at a second transfer gate (4) a corresponding first transfer gate control connection is connected with the first clock input (9a) of the clock receiver circuit device (1), and a corresponding second transfer gate control connection, inverse in relation to the first transfer gate control connection, with the second clock input (8a) of the clock receiver circuit device (1),

- whereby corresponding further connections of the transfer gates 4, 5) are connected with each other and are - jointly - connected with a clock output (11b) for emitting a clock output signal (bout).

10. A semi-conductor component with a receiver, in particular a clock receiver circuit device (1) according to one of claims 1 to 9.